REMARKS

Claims 1-21 are pending in the above-identified application. Claims 1-4, 6 and 8 are amended. Claims 11-21 are withdrawn.

The specification was objected to because the title of the invention was not descriptive. As shown above, applicants amend the specification to delete the old title and add a new title.

Claims 1-4 and 10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As the Examiner believes, "the active layer" in lines 7-8 in claim 1 should be "the active region." Accordingly, claim 1 is amended so that "the active layer" in lines 7-8 is replaced with "the active region."

The amendment to claim 3 simply changes the dependent form into the independent form. The same informality in connection with the active region is rectified in amended claim 3.

It is believed that the amended claims are in full compliance with 35 U.S.C. §112.

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Ichinose et al (U.S. Patent Application No. 2004/0009636 A1). The Examiner argues that Figure 13 of Ichinose et al. discloses that a device similar to the semiconductor device according to claim 1. However the present invention according to amended claim 1 is different from Ichinose et al. in light of the following matters.

The second silicon layer in claim 1 is different from silicon layer(s) in Figure 13 of Ichinose et al. In amended claim 1, the second silicon layer corresponds to the silicon

layer originally described in claim 1, while the first silicon layer, which is newly added, corresponds to the Si cap layer 35 in the first embodiment.

It is disclosed in Figure 13 of Ichinose et al. that a single crystal Si layer 1c is epitaxially grown over a SiGe layer 1b and a single crystal Si film 3 is epitaxially grown over the Si layer 1c and the SiGe layer 1b of the side walls of the groove. It is evident that two distinct Si layers (1b and 3) are formed in Ichinose et al., the former being formed on the SiGe layer 1b and the latter being formed on the side walls of the groove independently of the formation of the former.

Compared with Ichinose et al. in which the two distinct Si layers are formed independently, the single continuous second silicon layer is formed on the side wall of the element isolation groove and the SiGe layer in the active region in the present invention according to claim 1. In the point that the only single second silicon layer is formed continuously both on the side wall of the groove and the SiGe layer in the active region, the present invention according to claim 1 is substantially different from the device disclosed in Ichinose et al.. This technical feature is definitely claimed by the expression of "...a second silicon layer formed on. . . ." in claim 1.

In addition, as discussed in detail in the following argument regarding the claim rejection based on Ohnishi et al. (U.S. Patent Application No. 2004/0121554 A1), the present invention according to amended claim 1 has a technical feature that the first silicon layer and the second silicon layer are formed in the active region. Ichinose et al. fails to disclose or suggest the combined structure of the first silicon layer and the second silicon layer in the active region.

Thus, as argued above, the present invention according claim 1 is different from Ichinose et al. and is not anticipated by Ichinose et al.

Claims 1, 2, 4 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ohnishi et al. The Examiner argues that Figures 1-8, Figures 9-15 and Figures 16-21 of Ohnishi et al. disclose a semiconductor device similar to the semiconductor device according to claim 1. However, none of the sets of Figures of Ohnishi et al. discloses all the features of the present invention according to amended claim 1 as described below.

The present invention according to amended claim 1 has a technical feature that two silicon layers are formed over the SiGe layer in the active region. That is, the present invention according to amended claim 1 is characterized in that the first silicon layer is formed on the SiGe layer in the active region, and the second silicon layer is formed on the side wall of the element isolation groove and the first silicon layer in the active region.

The newly added first silicon layer corresponds to the Si cap layer 35 in the first embodiment (see page 15, the first to third paragraph of page 16, and FIGs. 2A-2B). As described in the specification, the Si cap layer 35 may be left on the SiGe buffer layer 12 in the active region 18 as shown in the attached FIGs. 1 and 2C, while the Si cap layer 35 is omitted in the original FIGs. 1 and 2C. It is obvious that the first silicon layer is also strained as the second silicon layer is strained.

It is clear that none of the sets of figures of Ohnishi et al. discloses both of the first and second silicon layers in the present invention according to claim 1. In Ohnishi et al. there is no strained Si layer on the SiGe layer from the beginning, and as a result when the Si layer is formed on the side wall of the groove of the SiGe layer and on the SiGe layer in the active region after forming the element isolation groove, the thickness of the

Si layer on the side wall of the groove is almost the same as that of the Si layer on the SiGe layer in the active region.

In the present invention according to claim 1, the whole thickness of the silicon layer(s) on the SiGe layer in the active region is thicker than that of the silicon layer on the side wall of the groove since the first silicon layer and the second silicon layer are formed on the SiGe layer in the active region, while only the second silicon layer is formed on the side wall of the groove. The present invention having such a structural feature makes it possible not only to suppress the generation of leak current at the side wall of the element isolation groove but also to additionally increase the thickness of the strained silicon layer on the SiGe layer in the active region with only one time CVD deposition of Si, while a strained silicon layer is originally formed only in a thickness below 20 nm due to its critical thickness. The present invention according to claim 1 can compensate the loss in the thickness of the silicon layer on the SiGe layer in the active layer due to the oxidation process, etc. As mentioned, the present invention has an advantage over Ohnishi et al and Ichinose et al. as well that the increase in the whole thickness of the strained silicon layer and the improvement of the yield can be realized without the increase of costs due to the complication of the fabrication process.

As discussed above, Ohnishi et al. does not disclose all the features of the present invention according to claim 1. Thus, claims 1, 2, 4 and 10 of the present invention are not anticipated by Ohnishi et al.

In view of the remarks above, Applicant now submits that the application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is believed that this application is not now in condition for allowance,

the Examiner is invited to contact Applicant=s undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

In the event that this paper is not timely filed, Applicant petitions for an appropriate extension of time. The fees for such an extension, or any other fees which may be due, may be charged to Deposit Account No. 50-2866.

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Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Darrin A. Auito
Reg. No.: 56,024
Attorney for Applicant
Tel: (202) 822-1100
Fax: (202) 822-1111

Attachments: Figs. 1 and 2A-C
(Note: Drawings are for explanation only. Drawings are not replacements sheets.)

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